Ring Oscillator: Frequency and Power Consumption as a Function of Supply Voltage

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The operational purpose of a ring oscillator has been described. The power consumption as well as the voltage vs. frequency will be measured with the use of a complimentary metal oxide semiconductor (CMOS) inverter. Using simulating software, these values will be graphically and numerically displayed throughout the paper.

Keywords: Ring oscillator, CMOS inverter

1. Introduction

Ring oscillators are used in a variety of systems, including radio frequency (RF) and lightwave communication systems. Specific to the ELEC 5270 class Low Power Design of Electronic Circuits and our study of transistor to transistor logic (TTL) in microelectronics, this study will focus on the use of a ring oscillator in a digital system. The most practical use of an oscillator in a digital system is for a time reference, also known as the clock signal. Ideally this creates a consistent periodic clocking point to signal the circuit to accept its next reading of its input and output (I/O) states of each logic gate. At each rise or ‘1’ the logic gates assigned to the respective oscillator or clock will accept their inputs and generate an output according to the inputs.

Depending on the application of the ring oscillator, the requirement on accuracy and stability will depend on the user’s acceptable range of error and other factors including outside noise, etc. Crystal Oscillators are used at the highest end of this demand because of their stability and frequency accuracy. While a benefit of these is the previously stated stability and accuracy, this is slightly offset by its high cost as well as its speed limitation. For the purposes of this exercise I will focus on the 32nm technology which was the dominant technology between 2010 and 2012 when it was replaced by 22nm technology.

A ring oscillator is composed of an odd number of inverting CMOS gates (or ‘NOT’ gates for logic purposes). The input is either a ‘High’ or ‘Low’ reading, and the output is the opposite of the input ‘High’ or ‘Low’. These high and low levels represent a digital 1 or 0, and the output of the chain is fed back into the input of the first gate. This paper will report its power and frequency performance as a function of the input voltage. It is important to note that the input voltage due to the design of the oscillator will be equal to VDD in the generated simulation. This will be illustrated further into this document. Input voltage (VDD) as well as the number of inverting gates will be altered, which should in theory be proportional to the delay. Other effects of these changes will be discussed in more depth in further sections. A very basic schematic of a ring oscillator can be seen below.



Fig. 1: 3 stage ring oscillator

Important benefits of a ring oscillator to remember:

1. Easily designed with Integrated Circuit (IC) technology
2. Can achieve oscillations at low voltage
3. Provides high frequency oscillations with dissipating low power
4. It can be electrically tuned
5. Provides a wide tuning range
6. It can provide multiphase outputs because of their simplistic structure.

For this exercise the most critical points to remember are 2 and 3, which will can be deduced from the simulation results.

## **Software Construction of an n-gate Ring Oscillator**

\*It is important to note for future reference that using Multisim software, the results generated were only ideal. A square wave was generated representing instantaneous transitions from low to high state and vice versa. Even with a varying number of gates used any noticeable delay was not detected on a graphical representation of the voltage over time. LTspice was chosen as a suitable software for its capability as well as its (from theoretical expectations) realistic results

Using LTspice the NOT gate was constructed by creating a CMOS gate using a PMOS and NMOS transistor. After inserting proper values for the transistors’ width and length as well as designating nodes as Input, Output, VDD and ‘GND’ a symbol for the NOT gate or inverter was created. Simulations using the default NOT gate provided results, however it was important to use the correct technology. This was done by using a text file provided by LTspice that was imported by assigning the transistors the corresponding name.



Fig. 2: CMOS Inverter LTspice

After creating the CMOS inverter, a representation was created for ease of use in recreating for a large chain of inverters.



Fig. 3: NOT Gate Representing CMOS Inverter

Ultimately put together the chain consisted of 5, 11, and 19 gates. VDD was varied between 0 and five volts, though values close to 0 will be disregarded because they either do not allow the NOT gate to change state, or increase the delay to an impractical number for the purposes of modern day computing.

Ultimately the design of the oscillator in the smallest design stage of this exercise (n=5 gates) is displayed in figure 4.



Fig. 4: LTspice Configuration



Fig. 5: TTL Representation Including Each Output

1. **Expected Results**

Given that ELEC 5270 is the first class I have taken that deals in some greater depth with microelectronics and integrated circuit technology, I think it is worth discussing the expected results in mathematical terms given our class material from this semester.

Power dissipation for each inverter will be calculated with the equation

 $∝\*f\*(Vdd)^{2}$ ……(1)

Where f is the observed frequency of the n-gate ring

 Given that n-gates are used, it should be the case that the power dissipation is directly proportional to the number of gates (n). Thus total power dissipation of the ring oscillator system can be written as

 $n\*∝\*f\*(Vdd)^{2}$ ……(2)

The delay of each gate can be represented by the equation

 $\frac{α\*Vdd}{(Vdd-Vth)}$ ……(3)

We can expect that the number of gates will be directly proportional to the resulting delay. An increase in Vdd should thus allow for a faster oscillation output.

The frequency of oscillation can be calculated by the equation.

 $\frac{1}{2nτ}$ ..….(4)

 Given these equations below are the following expectations made from initial observations.

Expectations:

1: Higher number of gates results in higher power consumption and lower frequency of oscillation

2: Higher Vdd results in higher frequency of oscillation

3: Lower Vdd results in power and frequency reduction

It is important to note in the third point that while the expected result of lower power consumption is ideal, it is possible that the lower frequency will render the system unpractical for some integrated circuit uses.

1. **Graphically Represented Results**

Recall that the number of inverters used was 5, 11, and 19. The results below will be given sequentially from the smallest number of inverters to the largest.

\*The minimum value of Vdd was determined to be .85 volts. Below this value resulted in significant delay or, at very low voltages, resulted in no oscillation. Also the maximum value used was 4 volts.

* 1. **Five Gate Ring Oscillator**

The configuration of the five ring oscillator was displayed in figure 4 in section 2. A transient sweep of 5 nanoseconds with 10 picosecond intervals was conducted. Below is the graphical result of two sweeps where Vdd was .85 and 2 volts respectively. The value of 2 volts was chosen because of its clear result. You will see that once we approach 2.5 volts and beyond, the high frequency generates incomplete transitions. Some of the results will be shortened from the entirety of the 5 nanosecond test, their trend is recognizable in a shorter amount of time.



Fig. 6: VDD=.85V (5 gates)



Fig. 7: VDD=2V (5 gates)

It is clear that a lower VDD results in a lower oscillation frequency.

**4.2 Trends in n-gate oscillators**

We should experience the same phenomenon in each of the cases, regardless of the number of gates. To confirm, the results of the 19 gate simulation is shown below in the identical case of VDD equal to .85 and 2 volts respectively. If this result confirms the expectations of section 3 and the results of 4.1, showing the graphical results of all n gate systems would be excessive when we can simply assume from the trends that they will be the same. The numerical result is the most valuable asset to this exercise.

Below is the result of the 19 gate ring oscillator system under the same circumstances of the 5 gate test; VDD=.85V and 2V respectively.



Fig. 8: VDD=.85V (19 gates)



Fig. 9: VDD =.85V (19 gates)

 Again the increase in voltage results in an increase in oscillation frequency. Of important note is the increased delay time given the increase in the number of gates. The output becomes less sinusoidal and begins to fit a more distinct square wave form.

Recall our expectations from section 3 above. This confirms the statement that higher number of gates results in an increase in delay which in turn decreases frequency. One result that was not anticipated was the square wave form taken on by the system with higher gates. Looking back this result is not out of the realm of possibility, rather one that was not considered before the simulation.

1. **Numerical Results of Simulation**

 Shown below are the numerical results of the simulation process. The results will be discussed in further detail in section 6, the conclusion.

 **5.1 5 Gate Ring Oscillator**

|  |  |  |
| --- | --- | --- |
| VDD (Volts) | Power (W) | Frequency (Hz) |
| 0.85 | .51u | 48M |
| 1 | 2.64u | 166M |
| 2 | 79u | 931M |
| 3 | 311u | 1.452G |
| 4 | .801m | 1.905G |

Fig. 10: 5 Gate System Results

 *At a glance* the results indicate that a higher VDD is directly proportional to an increase power and frequency. This is a trend that will continue for the 11 and 19 gate cases.

 **5.2 11 Gate Ring Oscillator**

|  |  |  |
| --- | --- | --- |
| VDD (Volts) | Power (W) | Frequency (Hz) |
| 0.85 | 1.02u | 29.1M |
| 1 | 5.85u | 105.4M |
| 2 | 171u | 625.1M |
| 3 | 685u | 987.2M |
| 4 | 1.59m | 1.294G |

Fig. 11: 11 Gate System Results

 **5.3 19 Gate Ring Oscillator**

|  |  |  |
| --- | --- | --- |
| VDD (Volts) | Power (W) | Frequency (Hz) |
| 0.85 | 1.87u | 20.8M |
| 1 | 9.89u | 73.5M |
| 2 | 300u | 370.2M |
| 3 | 1.16m | 571M |
| 4 | 2.79m | 698M |

Fig. 12: 19 Gate System Results

Section 5 is designated solely for the numerical representation of the simulation results for ease of reference. Section 6 will discuss the results in further depth.

1. **Numerical Result Analysis**

 In every case regardless of the number of gates, there is a very distinct relationship between VDD and the increase in power and frequency.

* 1. **Voltage vs. Power**

The numerical results of the power are plotted against voltage and each respective system in order to compare the relationship of VDD to power dissipation as well the relationship between power dissipation and number of gates.



Fig. 13: Power Consumption for n-gate Ring Oscillator

 When graphed, the results clearly indicate a clear relationship between VDD and power dissipation. Though in reality there is a limit on the value that VDD can take in an integrated circuit system, even within the range of 0.85 Volts to 4 Volts VDD, it can be said that there is an exponential relationship between the input power and power dissipation. Confirming our expectations from section three, it is clear that a higher value for VDD results in a higher value of power dissipation. Though the equation is not derived here, the exponential clearly would increase by some factor related to n, the number of gates.

 At the maximum tested VDD value of 4 volts there is a 71% decrease in power consumption between the 19 and 5 gate systems. Between the 19 and 11 gate system there is a 43% reduction in power consumption. Between the 11 and 5 gate system there is a 49% reduction in power consumption.

 If you observe the points where VDD has a value of 3 volts, there is a 41% decrease in power from the 19 gate system to the 11 gate system which is very nearly the 43% calculated for the value of VDD equal to 4 volts. Before making a definitive statement, the relationship of the VDD voltage to frequency has to be analyzed to see if this relationship holds.

 **6.2** **Voltage vs. Frequency**

The numerical results of the frequency are plotted against voltage and each respective system in order to compare the relationship of VDD to frequency as well the relationship between frequency and number of gates.



Fig. 14: Frequency for n-gate Ring Oscillator

 Though the initial transition from 0.85 to 1 volts slightly distorts the overall shape of the graph, it appears that the frequency takes the form of a logarithmic function when compared to the voltage VDD.

 From the value VDD equal to 4, there is a decrease in the frequency of 32% from the 19 gate system to the 11 gate system. From the 11 gate system to the 5 gate system there is a 46% decrease. From the 19 gate system to the 5 gate system there is a 63% decrease in frequency.

* 1. **Final Observations and Applications**

Though initially it appeared that the voltage and frequency were directly proportional to each other (section 5.1), when viewing the graphical results, it is clear that to say they are *directly* proportional to each other would be incorrect.

Depending on the requirements of the system there are advantages and disadvantages to each system and value of input voltage VDD. If speed is your primary concern, then it would be practical to prefer a low gate, high input voltage system. Though strictly in terms of power consumption and frequency it is the best system, it cannot be said that it is always the most practical to use. As mentioned above in section 1, the stability of the clock can be critical to a system as well. For instance if you were making constant measurements in extremely small time intervals (in nano or picoseconds), it may be critical to put more emphasis on the stability of the system. As we saw in figures 8 and 9 above, the high gate system results in a much more distinct square wave that has clear high and low levels. The lower gate system appeared to be a more sinusoidal, which would be more prone to distortion from noise as opposed to a purely square wave.

**References**

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